CS 314: TESTING OF DIGITAL SYSTEMS (3-1-0: 4)

Introduction and Fault Modeling
Introduction to testing. Difference between testing, fault diagnosis and verification.
Physical faults and their modelling: stuck-at faults, bridging faults, CMOS stuck-open and stuck-on faults.
Fault collapsing: fault equivalence and fault dominance.

Logic and Fault Simulation
Logic simulation techniques: compiled code, event-driven simulation.
Fault simulation techniques: parallel, deductive and concurrent fault simulation, critical path testing.

Automated Test Pattern Generation
Deterministic test generation for combinational circuits: Boolean difference method, path sensitization method, D-algorithm, PODEM, etc. Exhaustive and pseudo-exhaustive test pattern generation. Pseudo-random test pattern generation. Linear feedback shift register (LFSR), characteristic polynomial. Weighted random pattern generation.
Test generation for sequential circuits: time frame expansion method.

Design for Testability (DFT)
Test pattern generation for sequential circuits: adhoc and structured techniques. Scan path and level sensitive scan design (LSSD). Boundary scan (JTAG) standard.

Built-in Self-test (BIST)
Response compression techniques: ones count compression, transition count compression, signature compression. Aliasing and effects on fault coverage. BIST architectures: BILBO, STUMPS, etc.

Miscellaneous / Additional Topics in Testing
PLA testing: cross-point fault model. Test generation. Easily testable designs.
Memory testing: permanent, intermittent and pattern sensitive faults. Test generation: faults models, March tests.
System-on-chip (SoC) testing: soft, firm and hard cores, test wrapper, 1500 standard, Power aware testing.

Text Books

1. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing”, Kluwer Academic Publishers
2. N.K. Jha and S. Gupta, “Testing of Digital Systems”, Cambridge University Press

Reference Books

1. M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems Testing and Testable Design”, Wiley-IEEE Press
2. P.H. Bardell, W.H. McAnney and J. Savir, “Built-in Test for VLSI: Pseudorandom Techniques”, Wiley Interscience.
3. P.K. Lala, “Fault Tolerant and Fault Testable Hardware Design”, Prentice-Hall International

Prerequisite: CS 204: Computer Organization & Architecture