CS 413: High Performance Architectures (3-0-0: 3)

Review of Basic Organization and Architectural Techniques

RISC processors, Characteristics of RISC processors, RISC vs. CISC, Classification of instruction set architectures, Review of performance measurements, Basic parallel processing techniques: instruction level, thread level and process level.

Instruction Level Parallelism

Basic concepts of pipelining, Arithmetic pipelines, Instruction pipelines, Hazards in a pipeline: structural, data and control hazards, Overview of hazard resolution techniques, Dynamic instruction scheduling, Brach prediction techniques, Instruction-level parallelism using software approaches, Superscalar techniques, Speculative execution, Case study: Intel family of processors.

Multi-Processors

Centralized vs. distributed shared memory, Interconnection topologies, Multiprocessor architecture, Symmetric multiprocessors, Cache coherence problem, memory consistency, Multicore architecture, Case study: multiprocessors, co-processors like GPU.

Process Level Parallelism

Distributed Computers, Clusters, Grid

Text Books:

1. Hennessey and Patterson, “Computer Architecture: A Quantitative Approach”, Morgan Kaufman.

References:

1. K. Hwang, F. A. Briggs, “Computer architecture and parallel processing”, McGraw-Hill.
2. “Intel® 64 and IA-32 Architectures Optimization Reference Manual”, http://www.intel.com/content/www/us/en/architecture-and-technology/64-ia-32-architectures-optimization-manual.html
3. “Intel® 64 and IA-32 Architectures Software Developer Manuals”, http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
4. “Nvidia Kepler Compute Architecture White Paper”, http://www.nvidia.com/object/nvidia-kepler.html