	National Institute of Technology Meghalaya An Institute of National Importance		CURRICULUM
Programme	**Bachelor of Technology in Electrical and Electronics Engineering**	Year of Regulation	**2018-19**
Department	**Electrical Engineering**	Semester	**IV**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EE 218	**Digital Logic Design**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives	Course Outcomes	
To introduce the conversion technique of different number systems	CO1	Convert numbers from any number system or code to another
To make familiar with Boolean algebra, k-map, Quine Mcklusky and its uses for simplification of the expression	CO2	find out the simplest expression using Boolean algebra, K-map and Quine Mclusky method
To introduce different combinational and sequential logic circuit operation	CO3	understand and design logic circuit for combinational and sequential operation
To make familiar with the circuit operation of different logic gates	CO4	understand the circuit operation of any logic gate

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**3**	**3**	**2**									**1**	**1**	**0**	**0**
2	CO2	**3**	**3**	**2**									**1**	**2**	**1**	**1**
3	CO3	**3**	**3**	**3**	**2**								**1**	**2**	**1**	**0**
4	CO4	**3**	**1**	**3**									**1**	**1**	**1**	**1**

SYLLABUS

No.	Content	Hours	COs
I	**Boolean algebra and switching functions** Basic Logic Operation and Logic Gates, Truth Table, Basic Postulates and Fundamental Theorems of Boolean Algebra, Standard Representations of Logic Functions- SOP and POS Forms, Simplification of Switching Functions-K-Map and Quine-Mccluskey Tabular Methods, Synthesis of Combinational Logic Circuits.	**08**	**CO1**
II	**Combinational logic circuits using msi integrated circuits** Adder, Subtractor, BCD Adder, Parallel Binary Adder, Look Ahead Carry Adder, Encoder, Decoder, Multiplexer and Demultiplexer Circuits, Code converter, BCD-To-Segment Decoder, 7-Segment Displays..	**08**	**CO2**
III	**Introduction to flip-flops** Basic Concepts of Sequential Circuits, Cross Coupled SR Flip-Flop Using NAND or NOR Gates, JK Flip-Flop Rise Conditions, Clocked Flip-flops, D-Types and Toggle Flip-flops, Truth Tables and Excitation Tables for Flip-flop. Master Slave Configuration, Edge Triggered and Level Triggered Flip-flop, Elimination of Switch Bounce using Flip-flop, Flip-flop with Preset and Clear.	**07**	**CO3**
IV	**Sequential logic circuit design** Introduction to State Machine, Mealy and Moore Model, State Machine Notation, State Diagram, State Table, Transition Table, Table Excitation, Table and Equation, Basic Concepts of Counters and Register, Binary Counters, BCD Counters, Up Down Counter, Johnson Counter, Module-N Counter, Design of Counter using State Diagrams and Tables, Sequence Generators, Shift Left and Right Register, Registers with Parallel Load, Serial -in-Parallel-Out(SIPO) and Parallel-In-Serial-Out(PISO), Register Using Different Types of Flip-flop.	**08**	**CO3**
V	**Digital logic families** Digital IC Terminology, Transistor-Transistor Logic(TTL), Integrated Injection Logic(I2L), Emitter Coupled Logic (ECL), Metal Oxide Semiconductor(MOS) Logic, Complementary Metal oxide semiconductor (CMOS) Logic.	**05**	**CO3**
Total Hours		**36**	

Essential Readings

1. Floyed Thomas L. and Jain R. P., Digital Fundamentals, Pearson Education.

Supplementary Readings

1. Kime Charies R and Morris Mano, Logic and Computer Design Fundamentals, Pearson Education.
2. Mano Morris, Digital Logic and Computer Design, Pearson Education.
3. Jain R. P. and Anand M. H. S., Digital Electronics Practices using Integrated Circuits, TMH,
4. Lee Samual, Digital Circuits and Logic Design, PHI.