A TO THE OF TECHNOLOGY	Month B W. F.	National Institute of Technology Meghalaya An Institute of National Importance												CURRICULUM		
Programn	ne M a	aster of Computer Applications								Year of Regulation				2024-25		
Departme	ent Coi	mputer Scie	ence & Eng	gineering							Seme	ster			1	
Course Name					Dec December				Credit Structure				Marks Distribution			
Code		Course Name Pre-Requisi						e L	Т	Р	С	INT	MID	END	Total	
CA403		Computer Organization						3	0	0	3	50	50	100	200	
									CO's			ment		Bloom	s Taxonomy	
Course Objectives	COB1: To develop the student's ability to understand the concept of Instruction execution model, instruction set architecture and types, instruction formats and Addressing modes. COB2: To develop the student's ability to understand the concept of control unit CA403. Students should be able to Understand different functional units of a digital organized and design, performance strategies CA403. Students should be able to Solve th											of a digital co	omputer are hancement	understand Understand		
	design ba	design based on hardwired as well as micro-programmed control approach. 2 related problems of arithmetic logic ur virtual memory.											nit, cache and	ache and Evaluate		
		OB3: To provide the students with some knowledge and analysis skills ssociated with the design of Arithmetic and Logic unit.							CA403. 3	mapping techniques of cache memory, different adder circuits of ALU and different page replace algorithms of virtual memory.			, different	Analyse	Analyse	
	design, c	COB4: To develop the student's ability to understand the concept of memory design, cache memory and its mapping techniques and virtual memory. COB5: To provide the students with some basic knowledge of I/O mapping and control, interrupt and DMA mechanism.							CA403. 4				and I/O	Analyse		
Cos					Mapping	g with F	Program Ou	tcomes (PO	s)				Мар	Mapping with PSOs		
Cos	PO1	PO2	PO3	PO4	PO5	PO	9 PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	
CA403.1	3	1	1					1	1			2		1	3	
CA403.2	3	3	2	2	2			1	1			2	1	1	3	
CA403.3	3	3	3	2	2			2	2			2	2	2	3	
CA403.4	2	2	3		2	2	3		2			1	2	3	2	
CA403	2.75	2.25	2.25	2	2.00	2.00		1.33	1.5			1.75	1.67	1.75	2.75	
No.								/LLABUS					Hours		Cos	
Overview: (Hrs.: 6)		Content Block diagram of a computer system											03	CA403.1		
		Instruction execution model.											03	CA403.1		
Process	or	Instruction set architecture- types, formats, addressing modes Data path organization, Control unit design - Hardwired control, Microprogramming.											03	CA403.1 & CA403.2 CA403.1 & CA403.2		
Organization: (Hrs.: 10) Arithmetic and Logic unit: (Hrs.: 9)		CISC and RISC architecture, Instruction pipelining.											03		.1 & CA403.2	
		Computer arithmetic- Review of addition and subtraction											03	CA403.1, CA403.2 & CA403.3		
		Multiplio	Multiplication- Booth's, Array; Division- Restoring and non-restoring												CA403.1 & CA403.2	
			point arith			_							03	CA403.1 & CA403.2		
Memory Organization: (Hrs.: 10)		Interfacing of memory with processor, Memory hierarchy, Multiple-module memory,											04	CA403.1		
		Cache memory, Virtual memory.											06	CA403.1, CA403.2 & CA403.3		
Input/out	tput	Synchro	Synchronization of data transfer- strobed and handshaking;												A403.4	
Organization: (Hrs.: 7)		I/O mapping and control- Program controlled, Interrupt driven, DMA, Interrupt and DMA mechanisms.											04	CA403.4		
		Total Hours											42			
Essential F	Reading	s							·							
1. Ham	acher, C	arl, Zvonko	Vranesic,	and Safwa	t Zaky. <i>Con</i>	nputer o	rganization. N	/lcGraw-Hill, 2	002.							

2. Bryant, Randal E., O'Hallaron David Richard, and O'Hallaron David Richard. Computer systems: a programmer's perspective. Vol. 2. Upper Saddle River: Prentice Hall, 2003.

3. Stallings, William. *Computer organization and architecture: designing for performance*. Pearson Education India, 2003.

3. Ramachandran, Umakishore. *Computer systems: An integrated approach to architecture and operating systems*. Pearson Education India, 2011.

1. Hennessy, John L., and David A. Patterson. Computer architecture: a quantitative approach. Elsevier, 2011.

Supplementary Readings