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Progr	amme	COB1: To concept o and its pe COB2: To fundamen apply differed COB3: To analysis skeet technique COB4: To concept o coherence COB5: To distribute PO1	Academic Year of Regulat											2024-25	
Department Com			omputer Science and Engineering Semester									V			
Cours		Course Name F					Pre-Requisite	Credit St		tructure		Marks Distribution		n	
Code		High Performance Computing					Fie-Nequisite	L	Т	Р	С	INT	MID	END	Total
CA681	1							3	0	0	3	50	50	100	200
					.,				CO's	1 411 1	State			Bloom	's Taxonom
Course Objective	co an	COB1: To develop the student's ability to understand the concept of reduced and complex instruction set architecture and its performance. COB2: To develop the student's ability to understand the									les and	Understand			
	fur ap CC se an	fundamentals of pipelining, identify the cause of hazards and apply different approaches for possible hazard free solutions. COB3: To provide the students with some knowledge and analysis skills associated with the principles of superscalar							CA681.2	Able to understand the multiprocessor architecture, distributed memory architecture and distributed systems. Able to solve the performance related problems of pipeline structures, interconnect networks and memory. Able to analyze the performance differences of computing evolution on pipeline structures, interconnect networks, memory and distributed memory architecture			Understand		
	со	COB4: To develop the student's ability to understand the concept of shared- memory, distributed-memory, cache coherence problem and multiprocessor architecture.							CA681.3				ıres,	Evaluate	
		COB5: To provide the students with some basic knowledge of distributed system with its design principles.							CA681.4				evolution erconnect	Analyse	
						Mapping v	with Program Out	comes (POs	s)	.	•		Мар	Mapping with PSOs	
COs	P	PO1	PO2	PO3	PO4	PO5	PO6 PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CA681		3	1	1				1	1			2		1	
CA681			3	2	2	2		1	1			2	1	1	
CA681			3	3	2	2		2	2			2	2	2	
CA681		3	3	3	2	2		2	2			2	2	2	
CA68	1 3	3.00	2.5	2.25	2.00	2.00		1.5	1.5			2.00	1.67	1.5	
No.								LLABUS					Houro		<u></u>
ı	and its i	Content Hours Program execution: Program, Compilation, Object files, Function call and return, Address space, Data and its representation Computer organization: Memory, Registers, Instruction set architecture, Instruction processing								COs CA681.1					
	Pipelined processors: Pipelining, Structural, data and control hazards, Impact on programming Virtual memory: Use of memory by programs, Address translation, Paging								10	CA681.2, CA681.3					
	Cache memory: Organization, impact on programming, virtual caches Operating systems: Processes and system calls, Process management								10	CA681.3, CA681.4					
	Program profiling, File systems: Disk management, Name management, Protection, Parallel architecture: Inter-process communication, Synchronization, Mutual exclusion, Basics of parallel architecture, Parallel programming with message passing using MPI									CA681.2, CA681.4					

Essential Readings

- 1. J. L. Hennessy and D. A. Patterson, "Computer Architecture: A Quantitative Approach", 6th Edition, Morgan Kaufmann, 2017.
- 2. A. Silberschatz, P. B. Galvin, G. Gagne, "Operating System Concepts", 9th Edition, John Wiley, 2013.
- 3. R. E. Bryant and D. R. O'Hallaron, "Computer Systems: A Programmer's Perspective", 3rd Edition, Prentice Hall, 2015

Total Hours

Supplementary Readings

- 4. Hwang, Kai, "Advanced Computer Architecture with Parallel Programming", 3rd Edition, McGraw-Hill, 2017.
- 5. "Intel® 64 and IA-32 Architectures Optimization Reference Manual", http://www.intel.com/content/www/us/en/architecture-and-technology/64-ia-32-architectures-optimizationmanual.html

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- "Intel® 64 and IA-32 Architectures Software Developer Manuals", http://www.intel.com/content/www/us/en/processors/architectures-softwaredevelopermanuals.html
- 7. Nvidia Kepler Compute Architecture White Paper", http://www.nvidia.com/object/nvidia-kepler.html