	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Bachelor of Technology in Computer Science & Engineering**	Year of Regulation	**2019-2020**
Department	**Computer Science & Engineering**	Semester	**IV**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
CS 202	**Computer Organization**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives	**COB1: To develop the student's ability to understand the concept of Instruction execution model, instruction set architecture and types, instruction formats and Addressing modes.**	Course Outcomes	CO1	Students should be able to Understand the how different functional units of a digital computer are organized and design, performance enhancement strategies that adopted in performance evolution of different components of computer, arithmetic logic design, cache memory and different I/O mechanism of data transfer.
	COB1: To develop the student's ability to understand the concept of control unit design based on hardwired as well as micro-programmed control approach.			
	COB3: To provide the students with some knowledge and analysis skills associated with the design of Arithmetic and Logic unit.		CO2	Students should be able to Solve the performance related problems of arithmetic logic unit, cache and virtual memory.
	COB4: To develop the student's ability to understand the concept of memory design, cache memory and its mapping techniques and virtual memory.			
	COB5: To provide the students with some basic knowledge of I/O mapping and control, interrupt and DMA mechanism.		CO3	Analyze the performance differences of different mapping techniques of cache memory, different adder circuits of ALU and different page replacement algorithms of virtual memory.

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	3	1	1	-	-	-	-	1	1	-	-	2	-	1	-
2	CO2	3	3	2	2	2	-	-	1	1	-	-	2	1	1	-
3	CO3	3	3	3	2	2	-	-	2	2	-	-	2	2	2	-

SYLLABUS

No.	Content	Hours	COs
Overview: (Hrs.: 4)	Block diagram of a computer system	**02**	**CO1**
	Instruction execution model.	**02**	**CO1**
Processor Organization: (Hrs.: 10)	Instruction set architecture- types, formats, addressing modes	**03**	**CO1 & CO2**
	Data path organization, Control unit design - Hardwired control, Microprogramming.	**04**	**CO1 & CO2**
	CISC and RISC architecture, Instruction pipelining.	**03**	**CO1 & CO2**
Arithmetic and Logic unit: (Hrs.: 8)	Computer arithmetic- Review of addition and subtraction	**03**	**CO1, CO2 & CO3**
	Multiplication- Booth's, Array; Division- Restoring and non-restoring	**03**	**CO1 & CO2**
	Floating point arithmetic	**02**	**CO1 & CO2**
Memory Organization: (Hrs.: 8)	Interfacing of memory with processor, Memory hierarchy, Multiple-module memory,	**02**	**CO1**
	Cache memory, Virtual memory.	**06**	**CO1, CO2 & CO3**
Input/output Organization: (Hrs.: 6)	Synchronization of data transfer- strobed and handshaking;	**02**	**CO1**
	I/O mapping and control- Program controlled, Interrupt driven, DMA, Interrupt and DMA mechanisms.	**04**	**CO1**
	Total Hours	**36**	

Essential Readings

1. Hamacher, Carl, Zvonko Vranesic, and Safwat Zaky. *Computer organization*. McGraw-Hill, 2002.
2. Mano, M. Morris. *Computer system architecture*. Prentice-Hall of India, 2003.
3. Stallings, William. *Computer organization and architecture: designing for performance*. Pearson Education India, 2003.

Supplementary Readings

1. Hennessy, John L., and David A. Patterson. *Computer architecture: a quantitative approach*. Elsevier, 2011.
2. Bryant, Randal E., O'Hallaron David Richard, and O'Hallaron David Richard. *Computer systems: a programmer's perspective*. Vol. 2. Upper Saddle River: Prentice Hall, 2003.
3. Ramachandran, Umakishore. *Computer systems: An integrated approach to architecture and operating systems*. Pearson Education India, 2011.