	National Institute of Technology Meghalaya An Institute of National Importance	CURRICULUM

Programme	**Bachelor of Technology in Computer Science Engineering**	Year of Regulation	**2019-2020**
Department	**Computer Science Engineering**	Semester	**IV**

Course Code	Course Name	Credit Structure				Marks Distribution		
		L	T	P	C	Continuous Evaluation	Quiz/Viva	Total
CS 252	**Computer Organization Lab**	**0**	**0**	**2**	**1**	**70**	**30**	**100**

Course Objectives	
	Connect the theory of computer organization with hardware
	To develop knowledge about ALU operations
	Apply fundamentals of digital design and extend the learning to design sequential circuits
	To apply the concept of memory design, cache memory and its mapping techniques and virtual memory.

Course Outcomes	
CO1	Able to understand different operations on number systems
CO2	Able to acquire knowledge about assembly language code
CO3	Understanding of addition and subtraction, Multiplication-Booth's, Array
CO4	Introduce basics Division- Restoring and non-restoring; Floating point arithmetic
CO5	Able to Designing Adder, Multiplier, ALU on a simulator.
CO6	Exhibit the design of Registers and Counters on a simulator.

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**3**	**3**	**0**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**3**	**0**	**3**
2	CO2	**3**	**3**	**0**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**2**	**0**	**2**
3	CO3	**2**	**3**	**3**	**1**	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**2**	**3**	**2**
4	CO4	**2**	**2**	**3**	**0**	**2**	**2**	**3**	**0**	**2**	**0**	**0**	**1**	**2**	**3**	**2**
5	CO5	**2**	**2**	**3**	**0**	**2**	**2**	**3**	**0**	**2**	**0**	**0**	**1**	**3**	**3**	**3**
6	CO6	**2**	**3**	**2**	**1**	**2**	**2**	**2**	**0**	**2**	**0**	**0**	**1**	**2**	**3**	**3**

SYLLABUS

No.	Content	Hours	COs
1	Computer arithmetic	**02**	**CO1** **CO2** **CO3** **CO4** **CO5** **CO6**
2	Addition and subtraction, Multiplication	**02**	
3	Booth's, Array	**02**	
4	Division- Restoring	**02**	
5	Non-restoring	**02**	
6	Floating point arithmetic.	**02**	
7	Designing Adder, Multiplier	**02**	
8	Design of Registers and Counters	**02**	
9	Designing memory unit on a simulator.	**02**	
10	Designing CPU on a simulator.	**02**	
	Total Hours	**20**	

Essential Readings

1. Hamacher, Carl, Zvonko Vranesic, and Safwat Zaky. *Computer organization*. McGraw-Hill, 2002.
2. Mano, M. Morris. *Computer system architecture*. Prentice-Hall of India, 2003.
3. Stallings, William. *Computer organization and architecture: designing for performance*. Pearson Education India, 2003.

Supplementary Readings

1. Hennessy, John L., and David A. Patterson. *Computer architecture: a quantitative approach*. Elsevier, 2011.
2. Bryant, Randal E., O'Hallaron David Richard, and O'Hallaron David Richard. *Computer systems: a programmer's perspective*. Vol. 2. Upper Saddle River: Prentice Hall, 2003.
3. Ramachandran, Umakishore. *Computer systems: An integrated approach to architecture and operating systems*. Pearson Education India, 2011.