	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Bachelor of Technology in Computer Science & Engineering**	Academic Year of Regulation	**2018-19**
Department	**Computer Science & Engineering**	Semester	**VII**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
CS 419	**High Performance Architecture**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives	**COB1:** To develop the student's ability to understand the concept of reduced and complex instruction set architecture and its performance.	**Course Outcomes**	CO1	Able to understand the computer architectural design principles and performance enhancement strategies that adopted in performance evolution of different components of computer, multiprocessor architecture and distributed memory architecture and distributed systems.
	COB2: To develop the student's ability to understand the fundamentals of pipelining, identify the cause of hazards and apply different approaches for possible hazard free solutions.			
	COB3: To provide the students with some knowledge and analysis skills associated with the principles of superscalar technique and speculative execution.		CO2	Able to solve the performance related problems of pipeline structures, interconnect networks and memory.
	COB4: To develop the student's ability to understand the concept of shared-memory, distributed-memory, cache coherence problem and multiprocessor architecture.			
	COB5: To provide the students with some basic knowledge of distributed system with its design principles.		CO3	Able to analyze the performance differences of computing evolution on pipeline structures, interconnect networks, memory and distributed memory architecture

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	3	1	1	-	-	-	-	1	1	-	-	2	-	1	-
2	CO2	3	3	2	2	2	-	-	1	1	-	-	2	1	1	-
3	CO3	3	3	3	2	2	-	-	2	2	-	-	2	2	2	-

SYLLABUS

No.	Content	Hours	COs
Module 1: Review of Basic Organization and Architectural Techniques	RISC processors, Characteristics of RISC processors, RISC vs. CISC, Classification of instruction set architectures.	**02**	**CO1**
	Review of performance measurements, Basic parallel processing techniques: instruction level, thread level and process level.	**03**	**CO1, 2 & 3**
Module 2: Instruction Level Parallelism	Basic concepts of pipelining, Arithmetic pipelines, Instruction pipelines, Hazards in a pipeline: structural, data and control hazards.	**04**	**CO1**
	Overview of hazard resolution techniques, Dynamic instruction scheduling, Branch prediction, techniques and solution of its related problems. Instruction-level parallelism using software approaches.	**04**	**CO2**
	Job scheduling using reservation tables	**04**	**CO1, CO2, CO3**
	Superscalar techniques, Speculative execution, Case study: Intel family of processors.	**02**	**CO1**
Module 3: Multi-Processors	Understand and design of Centralized vs. distributed shared memory, Interconnection topologies.	**03**	**CO1,2 &3**
	Multiprocessor architecture, Symmetric Multiprocessors.	**03**	**CO1**
	Cache coherence problem, memory consistency.	**02**	**CO2&3**
	Multi-core architecture, Case study: multiprocessors, co-processors like GPU	**02**	**CO1**
Module 4: Process Level Parallelism	Distributed Computers, Clusters	**05**	**CO1**
	Grid Computing: understand features of grid computing and implement of it.	**02**	**CO1&2**
Total Hours		**36**	

Essential Readings

1. Hamacher, Carl, Zvonko Vranesic, and Safwat Zaky. *Computer organization*. McGraw-Hill, 2002 edition.
2. Hennessy, John L., and David A. Patterson. *Computer architecture: a quantitative approach*. Elsevier, 2011 edition.
3. Hwang, Kai, and Naresh Jotwani. *Advanced computer architecture, 3e*. McGraw-Hill Education, 2016 edition.

Supplementary Readings

1. Hwang, Kai. *Advanced Computer Architecture with Parallel Programming*. McGraw-Hill, 1993 edition.
2. "Intel® 64 and IA-32 Architectures Optimization Reference Manual", http://www.intel.com/content/www/us/en/architecture-and-technology/64-ia-32-architectures-optimizationmanual.html
3. "Intel® 64 and IA-32 Architectures Software Developer Manuals", http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
4. Nvidia Kepler Compute Architecture White Paper", http://www.nvidia.com/object/nvidia-kepler.html