to the second se
A MENTURE OF TECHNOLOGY HES

## National Institute of Technology Meghalaya

An Institute of National Importance

CURRICULUM

- OF IEGINA																			
Programme		ne	Bachelor of Technology in Electronics and Communication EngineeringYear of Regulation												2018-19				
Department			Electronics and Communication Engineering         Semester										ter	III					
Co	ourse				C	N					Credit St	ructure			Marks Distribution				
Code		Course Name								L	Т	Р	С	CONT EVAL	'INUOS JATION	VIVA Total		otal	
EC	253		Digital Logic Design Laboratory							0	1	2	2	,	70	30	30 100		
	To understand the principles of Boolean logic and optimize the circuits.							_	CO1	Able to understand the basic concepts of Boolean algebra and optimization of circuits.									
Co	ourse	To develop the skills for modular Boolean, Arithmetic and Sequential circuits CO2 To design combination								tional an	il and sequential circuits.								
Obje	ectives	To develop the student ability to design circuits using EDA tools Outcomes Able to predict a												ad analyse the behaviour of synchronous and					
	-	asynchronous circuits.																	
No.	COs		Mapping with Program Outcomes (POs)											Mapping		; with PSOs			
		PO	1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4	
1	CO1	3		2	3	1	-	-	-	-	-	-	-	-	3	-	-	-	
2	CO2	2		2	-	1	-	-	-	-	-	-	-	-	3	-	-	-	
3	CO3	3		3	2	1	2	-	-	-	-	-	-	-	2	3	-	-	
4	CO4	2		2	2	-	2	2	-	-	-	-	-	-	2	3	-	-	
NT								<u> </u>	5	YLLABUS									
NO.	Content													Hours		COs			
1	1 Implement half-adder/ half-subtractor circuits using a serial input.																		
2	Impler	nent full-	-adde	r/ full-su	btractor C	ircuits usi	ng a serial	input.											
							-	•											
3	Perfor	Perform 4-Bit Gray to Binary/ Binary to Gray code conversion using select input.																	
4	Perfor	rform and implement logic expression with the help of MUX IC 74153.																	
5	Imple	nplement the flip-flops using NAND/ NOR gate. 24															2, CO3		
6	Imple	Implement Excess-3 BCD adder/subtractor with select input.																	
7	Implei	Implement modulo-7 ripple counter.																	
8	Implement 4-bit shift left/right register.																		
9	Imple	ment the	e seal	llence ge	enerator														
10	Vorify	the beh				a and soo	upontial a	ironita nai	na ED/	A tools									
10	Total Hours														24				
Esse	ntial Re	adings																	
1. Mano Morris, Digital Logic and Computer Design, Pearson Education, 14 <sup>th</sup> ed. 2012.																			
2. A. Anand Kumar Fundamentals of Digital Circuits Prentice Hall India Learning, 4th ed. 2016.																			
3	3. D.V.	Hall, "D	Digital	l Circuits	and Syste	ems", Tata	u McGraw	Hill, 1 <sup>st</sup> ec	d., 1989.										
4	l. Char	les Roth,	, "Dig	gital Syst	em Desigr	n using VI	HDL", Tat	a McGraw	v Hill, 2 <sup>r</sup>	<sup>nd</sup> edition, 201	2.								

## **Supplementary Readings**

- 1. Brown S. and Zvonko Vranesic, Fundamental of Logic with Verilog Design, Tata McGraw Hill, 3<sup>rd</sup> Edition, 2013.
- 2. Kime Charies R and Morris Mano, Logic and Computer Design Fundamentals, Pearson Education, 4th Edition, 2013.