## National Institute of Technology Meghalaya

An Institute of National Importance

CURRICULUM

Γ	Programme		Bachelor of Technology in Electronics and Communication Engineering									Year of Re	egulation		2018-19	
Department		ent El	Electronics and Communication Engineering								Semester			VI		
Со	urse			C	ourse Nam	9				Credit	Structure			Marks D	istribution	
Code EC 302		Course Name						L	Т	Р	С	INT	MID	END	Total	
		Digital and Analog Integrated Circuits							3	1	0	4	50	50	100	200
		To understand the MOSFET structure and Operation								CO1	Model the behaviour of a MOS Transistor				r	
Course Objectives		To understand the CMOS differential Amplifier							Course	CO2	Design of MOS differential amplifier					
		To develop an ability of CMOS operational amplifier							Outcomes	CO3	Able to compute the MOS operational amplifier					
		To develop the CMOS digital circuits								CO4		•	IOS Invert			
										CO5	Able to analyse and design of CMOS digital circuits					S
No.	COs	Mapping with Program Outc							mes (POs)					pping with		
	005	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO
1	CO1	2	-	1	1	-	-	-	-	-	-	-	-	3	-	3
2	CO2	-	3	2	1	-	-	-	-	-	-	-	-	2	-	2
3	CO3	-	-	3	-	2	-	-	-	-	-	-	-	2	3	2
4	CO4	-	2	3	-	-	-	-	-	-	-	-	1	2	3	2
5	CO5	-	-	3	2	-	-	-	-	-	-	-	1	3	3	3
6	CO6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
								SYLLAE	BUS							
No.							Content							Hours		COs
I	MOS Transistor MOS Structure and Operation, MOSFET Structure And Operations, MOSFET Current- Voltage Characteristics, Channel Length Modulation, Substrate Bias Effect, MOSFET Capacitances, MOSFET Model.											h	10		CO1	
II	BJT/M Mirror	MOS Differential Amplifiers T/MOSFET Differential Amplifier, DC Transfer Characteristics of An Emitter-Coupled Pair / Source - Coupled Pair, Current irrors (Bipolar / MOS), Bipolar Widlar Current Source/ MOS Widlar Current Source, Cascaded Differential Amplifier Stages and evel Translator, AC and DC Analysis of Cascade Amplifier.									08		CO2			
III		Operational Amplifier FundamentalsOperational Amplifier, Basic Op-Amp Configuration, An Op-Amp with Negative Feedback, Voltage Series and Voltage Shunt arrations, Difference Amplifiers, Specification of An Op-Amp, Offset Voltages and Currents, CMRR, Slew Rate, PSRR, hcy Response, GBW Product, Input Bias and Offset Currents.06C														
	Config	urations, Di	fier, Basic C fference An	Dp-Amp Co plifiers, Sp	onfiguration pecification	of An Op-	-Amp, Offs							06	СС	)2, CO.
IV	Config Freque NMOS Resisti	urations, Di ncy Respon S Logic Des ve-Load Inv	fier, Basic C fference Am se, GBW Pr ign gerter, Satura	Dp-Amp Co nplifiers, Sp oduct, Inpu ated-Loade	onfiguration becification It Bias and d Inverter, 1	of An Op- Offset Cur Linear Loa	-Amp, Offs rents.	er, Depletio		nts, CMRI	R, Slew Ra	te, PSRR,		06		
	Config Freque NMOS Resisti VTC, C CMOS CMOS	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 5 Logic Des 6 Inverter Te	fier, Basic C fference Am se, GBW Pr ign gerter, Satura of VTC Crit ign	Dp-Amp Co nplifiers, Sp oduct, Inpu ated-Loaded ical Points, tatic Chara	nfiguration pecification It Bias and d Inverter, 1 Power Dis	of An Op- Offset Cur Linear Loa sipation ar	-Amp, Offs rents. Ided Inverte Id Rise Tin	er, Depletione - Fall Ti	es and Curren	nts, CMRI nverter, G Logic Gat	R, Slew Ra raphical De tes.	eterminatio	on of			)2, CO3
IV	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 6 Logic Des Inverter Te Gates, TTI	fier, Basic C fference Am se, GBW Pr ign verter, Satura of VTC Crit ign schnology, S L-CMOS Int	Dp-Amp Co plifiers, Sp oduct, Inpu ated-Loaded ical Points, tatic Chara erfacing.	nfiguration becification it Bias and d Inverter, Power Dis cteristics, I	of An Op- Offset Cur Linear Loa sipation ar	-Amp, Offs rents. aded Inverte ad Rise Tim ehavior, St	er, Depletione - Fall Ti	on Loaded In	nts, CMRI nverter, G Logic Gat er Dissipa	R, Slew Ra	eterminatio	on of	06		02, CO3 03, CO4 CO5
IV V	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS CMOS CMOS Fabrica Semico Type o	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 5 Logic Des 5 Inverter Te 6 Gates, TTI 5 Sing Techn ation Proces 5 Donductor M f Memories	fier, Basic C fference Am se, GBW Pr ign /erter, Satura of VTC Crit ign schnology, S -CMOS Int ology s Flow, CM	Dp-Amp Co nplifiers, Sp oduct, Inpu ated-Loaded ical Points, tatic Chara erfacing. OS N-Well ation Of R0	onfiguration pecification at Bias and d Inverter, T Power Dis cteristics, I Process, L OMs, MOS	of An Op- Offset Cur Linear Loa sipation ar Dynamic B ayout Desi ayout Desi ROM Cel eling of Se	-Amp, Offs rents. ded Inverte nd Rise Tim ehavior, St ign Rules, I ls, MOS El miconduct	er, Depletione - Fall Ti atic and Dy Full-Custor	on Loaded In ime, NMOS ynamic Pow	nts, CMRI nverter, G Logic Gat er Dissipa rout Desig	R, Slew Ra raphical Do tes. n, Stick Di ons, Static a	eterminatio	on of	06 08 04 06		)2, CO3 )2, CO3 )3, CO4 CO5 )2, CO4 CO4
IV V VI VII	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS CMOS CMOS Fabrica Semico Type o Read V	urations, Di ncy Respon S Logic Des ve-Load Inv Calculation S Logic Des Inverter Te Gates, TTI Sing Techn ation Proces onductor M f Memories Vrite Memo	fier, Basic C fference Am se, GBW Pr ign /erter, Satura of VTC Crit ign schnology, S -CMOS Int ology s Flow, CM	Dp-Amp Co nplifiers, Sp oduct, Inpu ated-Loaded ical Points, tatic Chara erfacing. OS N-Well ation Of R0	onfiguration pecification at Bias and d Inverter, T Power Dis cteristics, I Process, L OMs, MOS	of An Op- Offset Cur Linear Loa sipation ar Dynamic B ayout Desi ayout Desi ROM Cel eling of Se	-Amp, Offs rents. Ided Inverto Id Rise Tim ehavior, St ign Rules, I	er, Depletione - Fall Ti atic and Dy Full-Custor	es and Curren on Loaded In ime, NMOS ynamic Pow m Mask Lay	nts, CMRI nverter, G Logic Gat er Dissipa rout Desig	R, Slew Ra raphical Do tes. n, Stick Di ons, Static a	eterminatio	on of	06 08 04		)2, CO3 )3, CO4 CO5 )2, CO4
IV V VI VII Esser	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS CMOS CMOS Fabrica Semico Type o Read V	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 5 Logic Des 5 Inverter Te 5 Gates, TTI 5 Gates, TTI 5 sing Techn ation Proces 5 onductor M f Memories Vrite Memo	fier, Basic C fference Am se, GBW Pr ign /erter, Satura of VTC Crit ign schnology, S -CMOS Int ology s Flow, CM [emories , Implement ries, Organiz	Dp-Amp Complifiers, Spoduct, Input ated-Loadedical Points, tatic Charaerfacing. OS N-Well ation Of Ro	onfiguration becification at Bias and d Inverter, T Power Dis cteristics, I Process, L OMs, MOS AM, Parall	of An Op- Offset Cur Linear Loa sipation ar Dynamic B ayout Desi ayout Desi ROM Cel eling of Se Total	-Amp, Offs rents. ded Inverto d Rise Tin ehavior, St ign Rules, I ls, MOS El miconducto Hours	er, Depletione - Fall Ti atic and Dy Full-Custor PROM and or Memory	on Loaded In ime, NMOS ynamic Pow m Mask Lay d EEPROM	nverter, G Logic Gat er Dissipa rout Desig Applicatic Circuit Ch	R, Slew Ra raphical Detes. ation, Powe	eterminatio	on of roduct.	06 08 04 06		)2, CO3 )3, CO4 CO5 )2, CO4
IV V VI Zsser 1	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS CMOS Fabrica Semico Type o Read V tial Rea	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 6 Logic Des 5 Inverter Te 6 Gates, TTI 5 sing Techn ation Proces 5 onductor M 6 Memories 7 Vrite Memo 6 dings 7 Kang and Y	fier, Basic C fference Am se, GBW Pr ign verter, Satura of VTC Crit ign chnology, S L-CMOS Int ology s Flow, CM (emories , Implement ries, Organiz	Dp-Amp Complifiers, Spoduct, Input ated-Loaderical Points, tatic Charaerfacing. OS N-Well ation Of Ro zation of Ro zation of Ro	onfiguration pecification at Bias and d Inverter, T Power Dis cteristics, I Process, L OMs, MOS <u>AM, Parall</u> igital Integr	of An Op- Offset Cur Linear Loa sipation ar Dynamic B ayout Desi ayout Desi ROM Cel eling of Se Total	-Amp, Offs rents. ded Inverte nd Rise Tim ehavior, St ign Rules, I ls, MOS El miconduct Hours hts: Analys	er, Depletione - Fall Ti ne - Fall Ti natic and Dy Full-Custon PROM and or Memory	es and Curren on Loaded In ime, NMOS ynamic Pow m Mask Lay d EEPROM y Integrated	nverter, G Logic Gat er Dissipa rout Desig Applicatic <u>Circuit Ch</u> IcGraw-H	R, Slew Ra raphical Detes. ation, Powe	eterminatio	on of roduct.	06 08 04 06		)2, CO3 )3, CO4 CO5 )2, CO4
IV V VI Zsser 1	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS CMOS Fabrica Semico Type o Read V tial Rea	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 6 Logic Des 5 Inverter Te 6 Gates, TTI 5 sing Techn ation Proces 5 onductor M 6 Memories 7 Vrite Memo 6 dings 7 Kang and Y	fier, Basic C fference Am se, GBW Pr ign verter, Satura of VTC Crit ign chnology, S L-CMOS Int ology s Flow, CM (emories , Implement ries, Organiz	Dp-Amp Complifiers, Spoduct, Input ated-Loaderical Points, tatic Charaerfacing. OS N-Well ation Of Ro zation of Ro zation of Ro	onfiguration pecification at Bias and d Inverter, T Power Dis cteristics, I Process, L OMs, MOS <u>AM, Parall</u> igital Integr	of An Op- Offset Cur Linear Loa sipation ar Dynamic B ayout Desi ayout Desi ROM Cel eling of Se Total	-Amp, Offs rents. ded Inverte nd Rise Tim ehavior, St ign Rules, I ls, MOS El miconduct Hours hts: Analys	er, Depletione - Fall Ti ne - Fall Ti natic and Dy Full-Custon PROM and or Memory	on Loaded In ime, NMOS ynamic Pow m Mask Lay d EEPROM	nverter, G Logic Gat er Dissipa rout Desig Applicatic <u>Circuit Ch</u> IcGraw-H	R, Slew Ra raphical Detes. ation, Powe	eterminatio	on of roduct.	06 08 04 06		)2, CO3 )3, CO4 CO5 )2, CO4
IV V VI VII <u>Csser</u> 1 2	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS CMOS CMOS Fabrica Fabrica Semico Type o Read V	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 6 Logic Des 5 Inverter Te 6 Gates, TTI 5 sing Techn ation Proces 5 onductor M 6 Memories 7 Vrite Memo 6 dings 7 Kang and Y	fier, Basic C fference Am se, GBW Pr ign verter, Satura of VTC Crit ign schnology, S CMOS Int ology s Flow, CM (emories , Implement ries, Organiz 7. Leblebici, gn of Analog	Dp-Amp Complifiers, Spoduct, Input ated-Loaderical Points, tatic Charaerfacing. OS N-Well ation Of Ro zation of Ro zation of Ro	onfiguration pecification at Bias and d Inverter, T Power Dis cteristics, I Process, L OMs, MOS <u>AM, Parall</u> igital Integr	of An Op- Offset Cur Linear Loa sipation ar Dynamic B ayout Desi ayout Desi ROM Cel eling of Se Total	-Amp, Offs rents. ded Inverte nd Rise Tim ehavior, St ign Rules, I ls, MOS El miconduct Hours hts: Analys	er, Depletione - Fall Ti ne - Fall Ti natic and Dy Full-Custon PROM and or Memory	es and Curren on Loaded In ime, NMOS ynamic Pow m Mask Lay d EEPROM y Integrated	nverter, G Logic Gat er Dissipa rout Desig Applicatic <u>Circuit Ch</u> IcGraw-H	R, Slew Ra raphical Detes. ation, Powe	eterminatio	on of roduct.	06 08 04 06		)2, CO3 )3, CO4 CO5 )2, CO4
VI VI VI <u>Ssser</u> 1 2	Config Freque NMOS Resisti VTC, C CMOS CMOS CMOS CMOS CMOS CMOS Fabrica Semico Type o Read V tial Rea S-M. B. Ra	urations, Di ncy Respon 5 Logic Des ve-Load Inv Calculation 5 Logic Des 5 Inverter Te 6 Gates, TTI 5 Sing Techn ation Proces 5 Onductor M 6 Memories 7 Vrite Memo 6 Memories 7 Vrite Memo 8 Mang and Y 7 zavi, "Desig 1 ry Reading	fier, Basic C fference Am se, GBW Pr ign verter, Satura of VTC Crit ign schnology, S CMOS Int ology s Flow, CM (emories , Implement ries, Organiz 7. Leblebici, gn of Analog	Dp-Amp Complifiers, Sp oduct, Inputated-Loaded ical Points, tatic Chara erfacing. OS N-Well ation Of Ro zation of Ro zation of Ro zation of Ro zation of Ro zation of Ro zation of Ro	enfiguration becification at Bias and d Inverter, T Power Dis cteristics, I Process, L OMs, MOS AM, Parall igital Integr tegrated Ci	of An Op- Offset Cur Linear Loa sipation ar Dynamic B ayout Desi ayout Desi ROM Cel eling of Se Total rated Circu rcuit" Tata	-Amp, Offs rents. ded Inverto d Rise Tim ehavior, St ign Rules, I ls, MOS El miconduct Hours its: Analys McGraw-I	er, Depletione - Fall Ti atic and Dy Full-Custor PROM and or Memory sis and Des Hill, 2rd Ea	on Loaded In ime, NMOS ynamic Pow m Mask Lay d EEPROM y Integrated sign", Tata N dition, 2017	nverter, G Logic Gat er Dissipa rout Desig Applicatic <u>Circuit Ch</u> IcGraw-H	R, Slew Ra raphical Detes. ation, Powe	eterminatio	on of roduct.	06 08 04 06		)2, CO3 )3, CO4 CO5 )2, CO4