National Institute of Technology Meghalaya

An Institute of National Importance

CURRICULUM

Program		Bachelor of Technology in Electronics and Communication Engineering Yea									Year of Re	gulation		2018-2019			
Departme		ent Electronics and Communication Engineering												ster		VI	
Course Code EC 352 Course Objectives		Course Norma									Credit	Structure			Marks Distribution		
									L	Т	Р	С	Continu Evaluatio	al V on	VIVA	Total	
		Digital and Analog Integrated Circuits Lab								0	1	2	2	70		30	100
		To understand Spice Simulation of Circuits								-	CO1	Design of circuits using Spice simulator					
		To understand the amplifier characteristics								-	CO2	Design o	f amplifie	r using Spi	ce simulato	or	
		To develop an ability of CMOS Circuits								Course Outcomes	CO3	Able to design of CMOS digital circuits Able to analyse CMOS Inverter					
		To develop the CMOS Circuits Layouts									CO4						
										-	CO5	Able toa	nalyse the	VTC and la	ayout of Cl	MOS inver	ter
											CO6						
No.	COs	Mapping with Program Outcor								comes (POs)	s (POs)				Map	Mapping with PSOs	
1		PO	01	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSC
1	CO1	2		-	1	1	-	-	-	-	-	-	-	-	3	-	3
2	CO2	-		3	2	1	-	-	-	-	-	-	-	-	2	-	2
3	CO3	-		-	3	-	2	-	-	-	-	-	-	-	2	3	
4	CO4	-		2	3	-	-	-	-	-	-	-	-	1	2	3	
5	CO5	-		-	3	2	-	-	-	-	-	-	-	1	3	3	3
0	000	-		-	-	-	-	-			-	-	-	-	-	-	-
Jo	Content												Hours				
NO.		Content														005	
Ι	Introd	duction to SPICE Circuit Simulator.													4	4 CO1	
II	Inverti Summ Integra	verting and Non-Inverting Amplifier. mming, Scaling and Averaging. tegrator and Differentiator													6	6 CO2	
III	Implementation of CMOS Inverter. Obtain & Plot Its Transfer Characteristics, Determine Noise Margins and Measure Propagation Delay. Realization of MOSFET Characteristics Using Circuit Simulator Characteristics and BSIM Models. Realization of CMOS logic Gates.														4 CO2, C		02, CC
IV	Realization of CMOS Half Adder & Full Adder Circuit.														2 CO2, CO		
V	Design	Design and Implement of 1-Bit RAM CELL using JK & SR Flip-Flop.														2 CO4, (
VI	Layout of CMOS Inverter and Parasitic Extraction and Obtain VTC of Extracted Net List														4	4 CO2, C	
							Total	Hours							22		

Essential Readings

- 1. S-M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, 3rd Edition, 2002
- 2. B. Razavi, "Design of Analog CMOS Integrated Circuit" Tata McGraw-Hill, 2rd Edition, 2017

Supplementary Readings

- 1. H. Taub and D. Schilling, "Digital Integrated Electronics", McGraw-Hill, International, 2017.
- 2. R. Jan, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson Education, 2nd Edition 1999.
- 3. S. Salivahanan S., "Linear Integrated Circuits", McGraw-Hill, 3rd Edition, 2018