	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Bachelor of Technology in Electronics and Communication Engineering**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**VIII**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 422	**Low power VLSI**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Preliminaries on Power dissipation		CO1	Able to understand basics of Power Dissipation.
	Fundamentals of low power circuits.		CO2	Able to learn low power circuit design.
	Basic synthesis for low power circuits.		CO3	Able to learn circuit level optimization.
	Basics of SRAM memory		CO4	Able to acquire knowledge on SRAM.
	Basics of design and test of low voltage circuits		CO5	Able to design low power circuit at submicron level.

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**3**	**3**	**-**	**1**	**-**	**-**	**-**	**-**	**2**	**-**	**-**	**-**	**3**	**-**	**3**
2	CO2	**3**	**3**	**-**	**1**	**-**	**-**	**-**	**-**	**2**	**-**	**-**	**-**	**2**	**-**	**2**
3	CO3	**2**	**3**	**3**	**1**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**2**	**3**	**2**
4	CO4	**2**	**2**	**3**	**-**	**2**	**2**	**3**	**-**	**2**	**-**	**-**	**1**	**2**	**3**	**2**
5	CO5	**2**	**2**	**3**	**-**	**2**	**2**	**3**	**-**	**2**	**-**	**-**	**1**	**3**	**3**	**3**

SYLLABUS

No.	Content	Hours	COs
I	**POWER DISSIPATION IN CMOS** Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFET , gate induced drain leakage– Power dissipation in CMOS : short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design.	**8**	**CO1**
II	**DESIGN OF LOW POWER CIRCUITS:** Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization : Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops : Self-gating Flip-flop, Varieties of Boolean Functions, Adjustable Device Threshold Voltage.	**10**	**CO2**
III	**SYNTHESIS FOR LOW POWER** Behavioral Level Transforms, Logic Level Optimization for Low power, Circuit Level Optimization	**04**	**CO2, CO3**
IV	**LOW POWER STATIC RAM ARCHITECTURES** Organization of a static RAM, MOS Static RAM Memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits, method for achieving low core voltages from a single supply.	**8**	**CO3, CO4**
V	**DESIGN AND TEST OF LOW VOLTAGE CMOS CIRCUITS** Circuit Design style, Leakage current in deep submicrometer transistors, Deep submicrometer device design issues, Low voltage circuit design techniques, Designing deep submicrometer ics with elevated intrinsic leakage, multiple supply voltages.	**6**	**CO4, CO5**
Total Hours		**36**	

Essential Readings

1. K. Roy and S. C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley and Sons, 3 rd Edition, 2009.
2. Jan Rabaey, Low Power Design Essentials, Springer Publications, 1 st Edition, 2009.

Supplementary Readings

1. Chandrakasan and R. Brodersen, Low-Power CMOS Design, IEEE Press, 1 st Edition, 1995.
2. Chandrakasan, Bowhill, and Fox, Design of High-Performance Microprocessors, IEEE Press, 1 st Edition, 2000.