	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Bachelor of Technology in Electronics and Communication Engineering**	Year of Regulation	**2018-2019**
Department	**Electronics and Communication Engineering**	Semester	**VII**

Course Code	Course Name	Pre-Requisite	Credit Structure				Marks Distribution		
			L	T	P	C	Continuous Assessment	VIVA	Total
EC 451	**Computing and Simulation Lab**		**0**	**1**	**2**	**2**	**70**	**30**	**100**

Course Objectives		Course Outcomes		
	To introduce HDL software		CO1	Able to acquire knowledge about IC design software's
	To introduce complex logic function using HDL		CO2	Able to acquire knowledge about realization of digital circuits using CMOS
	Introducing of short-time processing of speech signals and time-frequency analysis of speech signals		CO3	Able to design Digital gates using HDL
	Introducing of the fundamentals of ML techniques useful for speech processing applications		CO4	Able to design of Complex circuits using HDL
			CO5	Able to perform analysis of speech signals using time-frequency representation.
			CO6	Able to develop ML techniques for speech recognition, signal and source separation.

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**3**	**3**	-	**1**	-	-	-	-	**2**	-	-	-	**3**	-	**3**
2	CO2	**3**	**3**	-	**1**	-	-	-	-	**2**	-	-	-	**2**	-	**2**
3	CO3	**2**	**3**	**3**	**1**	**2**	-	-	-	-	-	-	-	**2**	**3**	**2**
4	CO4	**2**	**2**	**3**	-	**2**	**2**	**3**	-	**2**	-	-	**1**	**2**	**3**	**2**
5	CO5	**2**	**2**	**3**	-	**2**	**2**	**3**	-	**2**	-	-	**1**	**3**	**3**	**3**
6	CO6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

SYLLABUS

No.	Content	Hours	COs
1	Analysis of speech signals using time-frequency representation	**02**	**CO1** **CO2** **CO3** **CO4** **CO5**
2	Algorithms for acoustic signal processing	**02**	
3	Feature extraction for source separation	**02**	
4	Speech enhancement	**02**	
5	Speaker emotion recognition	**02**	
6	Introduction of HDL Software Tool.	**02**	
7	Implementation and Simulation of Logic Gate with HDL.	**02**	
8	Implementation of Digital Logic with Different Model of HDL.	**02**	
9	Design and Implementation of Arithmetic Building Blocks in FPGA.	**02**	
10	Design and Implementation of Array Building Blocks in FPGA.	**02**	
	Total Hours	**20**	

Essential Readings

1. M. Sarrafzadeh and C. K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill, 1st Edition, 1996
2. P. Ashenden, "Digital Design using VHDL", Elsevier, 1st Edition, 2007
3. J. R. Deller, Jr., J. H. L. Hansen and J. G. Proakis, "Discrete-Time Processing of Speech Signals", WileyIEEE Press, NY, USA.
4. C.M. Bishop, "Pattern Recognition and Machine Learning", 2nd Edition, Springer, 2011.

Supplementary Readings

1. P.J Anderson, "The designer's guide to VHDL", Morgan Kaufman, 1st Edition, 2008
2. N.H.E. Weste, K. Haase, D. Harris, A. Banerjee, "CMOS VLSI Design: A circuits and Systems Perspective", Pearson Education, 4th Edition, 2011
3. W.Wolf , "FPGA System design", Pearson, 1st Edition, 2004
4. D. Yu and L. Deng, "Automatic Speech Recognition: A Deep Learning Approach", Springer, 2016