| State NATIONAL | A TI B Z POP | And R R WAY HA | National Institute of Technology Meghalaya An Institute of National Importance | | | | | | | | | | | | | CURRICULUM | | |
|----------------------|--|---------------------------------------|---|------------------------------|--------------|--------------------|-------------|--------------|------------|--------------------|-------------|---------------------------------------|-----------|------|--------------------|-------------------|----------------|--|
| F | rogramn | ne | Bachelor of Technology in Electronics and Communication Engineering | | | | | | | | | Year of Regulation | | | | 2018-19 | | |
| Ι | Departme | nt | Elect | ronics an | d Commu | inication E | Ingineerin | g | | | | | Semester | | | VII | | |
| Co | urse | | Course Name | | | | | | | Credit | | Structure | | | Marks Distribution | | | |
| C | ode | | | | | | C | | | L | Т | Р | С | INT | MID | END | Total | |
| EC | 475 | 5 Basics of VLSI 2 0 0 | | | | | | | | | | | 2 | 50 | 50 | 100 | 200 | |
| | Preliminaries on MOS device CO1 Able to understand basics of | | | | | | | | | | basics of M | IOS. | | | | | | |
| Course Objectives | | Fundamentals of Digital Circuits. CO2 | | | | | | | | | | Able to learn basic Digital circuits. | | | | | | |
| | | Basic a | nalysis | $\frac{s \text{ of CMO}}{1}$ | S inverter | | | | | Course Outcomes | CO3 | Able to design CMOS inverter. | | | | | | |
| | | CMOS | comb | inational o | circuit desi | gn | | | | | CO4 | Able to design CMOS combination | | | ational circ | uits. | | |
| | - | | | | | | | | | | | | | | | | | |
| | | Manning with Program Outcomes (POs) | | | | | | | | | | | | | | Manning with PSOs | | |
| No. | COs | PO | 1 | PO2 | PO3 | PO4 | | PO6 | | | PO9 | PO10 | PO11 | PO12 | PSO1 | | PSO3 | |
| 1 | CO1 | 3 | | 3 | - | 104 | - | - | - | - | 2 | - | - | - | 3 | - | 3 | |
| 2 | CO2 | 3 | | 3 | _ | 1 | _ | _ | _ | _ | 2 | _ | - | _ | 2 | _ | 2 | |
| 3 | CO3 | 2 | | 3 | 3 | 1 | 2 | _ | _ | _ | - | _ | _ | _ | 2 | 3 | 2 | |
| 4 | CO4 | 2 | | 2 | 3 | - | 2 | 2 | 3 | - | 2 | - | - | 1 | 2 | 3 | 2 | |
| 5 | CO5 | - | | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| 6 | CO6 | - | | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| SYLLABUS | | | | | | | | | | | | | | | | | | |
| No. | Content | | | | | | | | | | | | | | Hours | | COs | |
| Ι | INTRODUCTION TO MOS DEVICE: First Glance at the MOS device MOS Transistor under static conditions, threshold voltage, channel length modulation. | | | | | | | | | | | | | | 4 | | CO1 | |
| II | DIGITAL LOGIC DESIGN Logic Gates, Boolean functions, AOI logic, Full adder design, Decoder, Multiplexer. | | | | | | | | | | | | | | 8 | 8 CO2 | | |
| III | INVERTER DESIGN: Static CMOS inverter, performance of CMOS inverter, propagation delay sizing inverter for performance. | | | | | | | | | | | | | | 04 | | CO2, CO3 | |
| IV | CMOS COMBINATIONAL LOGIC DESIGN: Static CMOS designs, complementary CMOS design, power consumption in CMOS logic gates, design techniques to reduce switching activity, pass transistor logic, differential pass transistor logic, dynamic CMOS design, Domino CMOS logic, NPCMOS- logic style. | | | | | | | | | | | | | | 8 | | 93, CO4 | |
| | | | | | | | Total | Hours | | | | | | | 24 | | | |
| Esser | ntial Rea | dings | | | | | | | | | | | | | | | | |
| 1 | . R. Jan, | Chandra | kasan | , and A. N | Nikolic, Di | gital Integr | ated Circui | its: A Desig | gn Perspec | tive, Pearso | n Educati | on 2nd edit | ion 2016. | | | | | |
| Supp | lementa | ry Read | lings | | | | | | | | | | | | | | | |
| 1. | S-M. 1 | Kang and | dY.L | eblebici, | CMOS Dig | gital Integra | ated Circui | ts: Analysi | is And Des | sign, Tata Mo | cGraw-Hi | ll, 3 rd edit | ion 2002. | | | | | |