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| | **National Institute of Technology Meghalaya**<br>An Institute of National Importance | **CURRICULUM** |

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|---|---|---|---|
| Programme | **Master of Technology in VLSI and Embedded Systems** | Year of Regulation | **2018-19** |
| Department | **Electronics and Communication Engineering** | Semester | **II** |

| Course Code | Course Name | Credit Structure | | | | Marks Distribution | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | L | T | P | C | INT | MID | END | Total |
| **EC 516** | **VLSI PHYSICAL DESIGN & AUTOMATION** | **3** | **0** | **0** | **3** | **50** | **50** | **100** | **200** |

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|---|---|---|---|---|
| Course Objectives | Understand Physical Design basic concepts of partitioning, Floor-planning, Placement and Routing | Course Outcomes | CO1 | Able to place and partition the blocks while for designing the layout for IC. |
| | Discuss the concepts of design optimization algorithms and their application to physical design automation | | CO2 | Able to solve the performance issues in circuit layout |
| | Realize the concepts of simulation and synthesis in VLSI Design Automation | | CO3 | Able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing |
| | Formulate CAD design problems using algorithmic methods | | CO4 | Able to analyze circuits using both analytical and CAD tools |

| No. | COs | Mapping with Program Outcomes (POs) | | | | | | | | | | | | Mapping with PSOs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 | |
| 1 | CO1 | **2** | **1** | **0** | **3** | **0** | **0** | - | - | - | - | - | - | **3** | **3** | **1** | |
| 2 | CO2 | **2** | **3** | **0** | **1** | **0** | **0** | - | - | - | - | - | - | **2** | **3** | **1** | |
| 3 | CO3 | **3** | **2** | **3** | **3** | **3** | **0** | - | - | - | - | - | - | **1** | **1** | **3** | |
| 4 | CO4 | **2** | **2** | **3** | **0** | **2** | **3** | - | - | - | - | - | -- | **0** | **1** | **1** | |

**SYLLABUS**

| No. | Content | Hours | COs |
|---|---|---|---|
| I | Data Structures and Basic Algorithms<br>Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical design | 8 | CO1,CO2 |
| II | Partitioning<br>Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms. Performance Driven Partitioning. | 8 | CO2,CO3 |
| III | Floor Planning, Pin Assignment & Timing<br>Floor planning, Chip planning, Pin Assignment Algorithms , Timing Concepts | 8 | CO3 |
| IV | Global Routing<br>Problem Formulation, Classification of Global Routing, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing. | 8 | CO2 |
| V | Detailed Routing<br>Problem Formulation, Classification of Routing Algorithms, Single-Layer Routing Algorithms, Two-Layer Channel Routing Algorithms, Three-Layer Channel Routing Algorithms, Multi-Layer Channel Routing Algorithms, Switchbox Routing Algorithms | 5 | CO3,CO4 |
| VI | Over-the-Cell Routing and Via Minimization<br>Over-the-cell Routing, Via Minimization. Clock and Power Routing: Clock Routing, Power and Ground Routing. Compaction: Problem Formulation, Classification of Compaction Algorithms, One-Dimensional Compaction, Two-Dimensional Compaction. | 4 | CO4 |
| | Total Hours | 41 | |

**Essential Readings**


1. N. Sherwani, Algorithms for VLSI Physical Design Automation, Springer Publications,1999.
2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, TMH, 1996
3. S. K. Lim, Practical Problems for VLSI Physical Design Automation, Springer Publications ,2008


**Supplementary Readings**


1. Hill & Peterson, Computer Aided Logical Design with Emphasis on VLSI , Wiley.1993.
2. W. Wolf, Modern VLSI Design: Systems on silicon, 4th edition, Pearson Education Asia ,1993