	National Institute of Technology Meghalaya An Institute of National Importance	CURRICULUM

Programme	**M.Tech/Ph.D**	Year of Regulation	**2022**
Department	**Electronics and Communication Engineering**	Semester	**I**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 539	**RTL Simulation and Synthesis with PLDs**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives	To provide students an understanding of the concepts related to RTL Designing	Course Outcomes	CO1	Able to gain insights into various RTL methodologies and HDL concepts
	To design and implement the architectures on FPGA		CO2	Able to model the combinational and sequential circuits on FPGA
	To familiarize students on timing concepts on FPGAs and ASICs		CO3	Able to implement the designs with area efficient Time efficient RTLs
	To understand the protocols and interface with FPGAs		CO4	Able to interface practical communication circuits with protocols and sensors

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	3	2	2	1	0	0	0	0	2	0	0	0	3	2	3	0
2	CO2	2	3	2	2	0	0	0	0	2	0	0	0	3	1	2	0
3	CO3	1	2	3	2	2	0	0	0	0	0	0	1	2	2	3	0
4	CO4	1	3	3	0	0	0	0	0	1	0	0	0	2	3	2	0

SYLLABUS

No.	Content	Hours	COs
I	**Logic Implementation and HDL** Digital system design options and trade-offs, Design methodologies, High Level System Architecture and Specification: Behavioural modelling and simulation using HDL Hardware description languages, combinational and sequential design, state machine design (synchronous and Asynchronous), High Performance and Low power design architectural solutions RTL synthesis issues, test benches	14	CO1
II	**FPGA Architecture & methodology** Overview of FPGA architectures, granularity of function and wiring resources, Logic block architecture: FPGA logic cells, timing models, power dissipation I/O block architecture: Input and Output cell characteristics, clock input, Timing, Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs, Power dissipation, Partitioning and Placement, Routing resources delays effects. Introduction to ASIC and Embedded system Design methods	10	CO2
III	**Protocols & Case studies** General purpose I/O Devices UART, I2C, SPI, LCD Protocols, DSP application case studies FFT, DCT, FIR Filter etc .	12	CO3
	Total Hours	36	

Essential Readings

1. Denmis silage , “Trends in Embedded Design Using Programmable Gate Arrays”,Edition -1 Bookstand Publishing Publications 2013
2. Majid Sarrafzadeh, C. K. Wong, “FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version”, Edition -1 Wiley-Interscience 2008
3. Peter Ashenden, Digital Design using Verilog, Elsevier, Edition -1 Publications, 2007
4. Sarah Harris, David Harris, “Digital Design and Computer Architecture, RISC-V Edition ”, MGH, International Editions, 2021
5. Sarah Harris Digital Design and Computer Architecture Edition -2 2016 Elsevier Morgan Kaufmann