TELEKINESIS

ELECTRONICS AND COMMUNICATION ENGINEERING
DEPARTMENT MAGAZINE

VOLUME IV
AUGUST 2025

National Institute of Technology Meghalaya

An Institute of National Importance

"Telekinesis"

"Telekinesis" combines "Tele," meaning "Distance," and "Kinesis," meaning "Movement" or "Motion."

Together, "Telekinesis" can be interpreted as "Movement at a Distance." It symbolizes the ability to control or influence from afar, aligning with the essence of electronics and communication engineering, where invisible signals, waves, and technologies bridge distances. The name suggests innovation, unseen power, and forward-thinking approaches in the field, making it a great name for this magazine that highlights the latest trends and breakthroughs in electronics and communication engineering.

Table Of Contents

About the Institute

The National Institute of Technology (NIT) Meghalaya is one of the thirty-one NITs in India established under the NIT Act 2007 (Amended 2012) of the Parliament of India as Institutes of National Importance with full funding support from the Ministry of Education (Shiksha Mantralaya), Government of India.

The Vision

A Centre of Excellence vibrant with academic activities and bubbling with youthful creative energy, making significant contributions to the World of Knowledge and Technology and to the Development of the State, the Region and the Nation.

The Mission

To impart quality education in the fields of engineering, science, and technology at undergraduate and postgraduate levels, with special attention to encouraging innovation and creativity in these fields in a clean and healthy environment.

About the Department

The Department of Electronics and Communication Engineering (ECE) was established in 2010 with the inception of the NIT Meghalaya. The department offers a B. Tech Programme with an intake capacity of thirty & an M. Tech Programme with an intake capacity of twenty in ECE and a Ph.D.Program in various specialized areas. The major research areas of the department include high-speed and low-power VLSI, Computer Arithmetic, Wireless Sensor Networks, Cognitive Radio, Antenna Design, and Signal Processing. The major objective of the Department is to impart high-quality technical education and research with a strong foundation in Electronics and Communication Engineering. The department's major areas of faculty expertise include VLSI Systems, High Performance Computing, Signal Processing, Digital Signal Processing, Communication, and RF & microwave engineering.

The Vision

A Centre of Excellence in knowledge and technological innovation research hub in the field of Electronics and Communication Engineering by the creation of skilled manpower to meet the local, national, and global needs of industry and society.

The Mission

- To impart research & training on cutting-edge technologies on VLSI, Signal Processing, and Communication for societal issues.
- To promote competitive academic programs through industry-relevant skills that support entrepreneurial growth and industry readiness.
- To strengthen moral values and ethics with managerial skills to become technocrats and entrepreneurs.

TECHNICAL Articles

Electronics and Communication Department

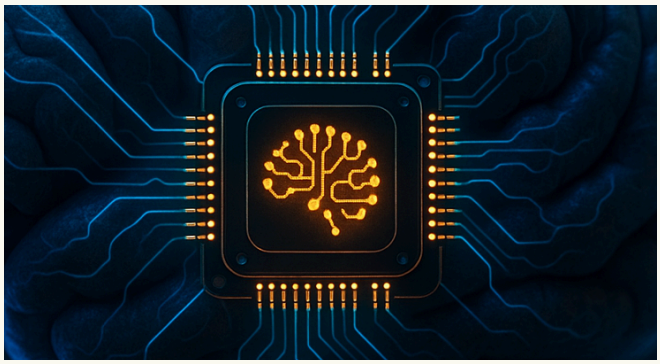
Brains on a Chip
Neuromorphic VLSI

M.A.SEENIVASAN, Research Scholar, ECE

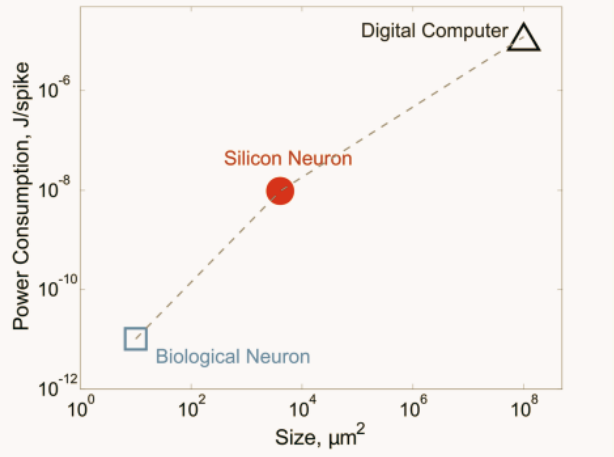
Brains on a chip

Long the stuff of science fiction, the concept of real "brains on a chip" has moved closer to reality with recent breakthroughs in neuromorphic engineering. By mimicking the architecture and function of the human brain, researchers are dev eloping Neuromorphic circuits that could revoli- tionize computing by providing specialized hardware for artificial intelligence (AI) applications.

Neuromorphic chips are modeled on biological brains and aim to replicate the operation of neurons and the adaptable synapses they engage. Signals are processed in parallel through of spiking neurons, a departure from conventional processors - and synaptic weights change in response to neural activity. This brain-inspired behavior enables capabilities such as learning from experience while consuming minimal power.



Next-generation large-scale iono-neuromorphic silicon neural networks:
From a neuroscience perspective, a fundamental drawback of such nano-sized neuronal analogs is that they are largely phenomenological (artificial) rather than iono-neuromorphic (realistic) models of neuronal function. Future neuromorphic modeling efforts should therefore target not only the integration density and computation and/or power efficiencies of the neuronal analogs (Figure 1) but also their degree of biological realism and robustness, if the full glory of the brain is ever to be captured on chip



Biological and silicon neurons have much better power and space efficiencies than digital computers. A biological neuron consumes approximately 3.84 × 108 ATP molecules in generating a spike (Attwell and Laughlin, 2001; Lennie, 2003). Assuming 30–45 kJ released per mole of ATP (Berg et al., 2007; or 5–7.5 × 10-20 J per ATP molecule), the energy cost of a neuronal spike is in the order of 10-11 J. The density of neurons under cortical surface in various mammalian species is 100,000/mm2 (Braitenberg and Schüz, 1998), which translates to a span of 10 μm2 per neuron. Silicon neurons have power consumption in the order of 10-8 J/spike on a biological timescale. For example, an Integrate-and-Fire neuron circuit consumes 3–15 nJ at 100 Hz (Indiveri, 2003) and a compact neuron model consumes 8.5–9.0 pJ at 1 MHz (Wijekoon and Dudek, 2008), which translates to 85–90 nJ at 100 Hz. For silicon neurons, the on-chip neuron area is estimated to be 4,000 μm2 (70 μm × 40 μm in Wijekoon and Dudek, 2008, 3750 μm2 in Vogelstein et al., 2007, and 70 μm × 70 μm in Wijekoon and Dudek, 2009). According to Liu and Delbrück (2007), digital computers are 104–108 less efficient than biological neurons. The power efficiency of digital computers is therefore estimated to be 10-3–10-7 J/spike. Most current multi-core digital microprocessor chips have dimensions from 263 to 692 mm2. A single core has an average size from 50 to 90 mm2.

Neuromorphic silicon neurons: state of the art

Complementary metal-oxide-semiconductor (CMOS) transistors are commonly used in very-large-scale-integration (VLSI) digital circuits as a basic binary switch that turns on or off as the transistor gate voltage crosses some threshold. Carver Mead first noted that CMOS transistor circuits operating below this threshold in current mode have strikingly similar sigmoidal current–voltage relationships as do neuronal ion channels and consume little power; hence they are ideal analogs of neuronal function (Mead, 1989). This unique device physics led to the advent of "neuromorphic" silicon neurons (SiNs) which allow neuronal spiking dynamics to be directly emulated on analog VLSI chips without the need for digital software simulation (Mahowald and Douglas, 1991). In the inaugural issue of this Journal, Indiveri et al. (2011) review the current state of the art in CMOS-based neuromorphic neuron circuit designs that have evolved over the past two decades. The comprehensive appraisal delineates and compares the latest SiN design techniques as applied to varying types of spiking neuron models ranging from realistic conductancebased Hodgkin–Huxley models to simple yet versatile integrate-and-fire models. The timely and much needed compendium is a tour de force that will certainly provide a valuable guidepost for future SiN designs and applications.

Neuromorphic Circuits: Brains on a Chip

Neuromorphic circuits emulate various neural functions, including spiking behavior, synaptic plasticity, and learning. These circuits are typically built using analog, digital, or mixed-signal approaches:

- Analog neuromorphic circuits replicate biological dynamics such as membrane potential and ion channel behavior with high energy efficiency, but face challenges in precision and variability.
- Digital neuromorphic systems (like Intel's Loihi or IBM's TrueNorth) offer scalability and programmability, albeit at a higher energy cost.
- Mixed-signal designs strive to capture the best of both worlds, using analog processing for spikes and digital for control and communication.

Systems and Applications

At the systems level, neuromorphic computing supports event-driven processing and edge AI—making it ideal for low-power applications like robotics, sensor networks, brain-machine interfaces, and even autonomous vehicles.

Examples of deployed systems include:

- Loihi 2 (Intel) for adaptive robotic control
- SpiNNaker (University of Manchester) for simulating large-scale neural networks
- BrainScaleS (Heidelberg University) for hybrid analog-digital emulation of brain circuits

Emerging research is exploring how these systems can learn in real-time, adapt to new environments, and even simulate neurological diseases for biomedical research.

Challenges Ahead

Despite the promise, neuromorphic computing faces significant hurdles:

- Standardization issues, due to diverse architectures
- Programming complexity, with no widely accepted neuromorphic language
- Integration with existing AI pipelines, which are largely optimized for GPU-based platforms

However, breakthroughs in materials (e.g., phase-change memory, ferroelectric transistors) and algorithms (like STDP and reinforcement learning) are steadily closing the gap between biological intelligence and silicon computation.

Intel's Hala Point: The World's Largest Neuromorphic System

Intel has developed Hala Point, the world's largest neuromorphic computing system. It integrates 1,152 Loihi 2 processors, simulating 1.15 billion artificial neurons and 128 billion synapses. This system achieves up to 20 quadrillion operations per second (20 petaops) with an energy efficiency exceeding 15 trillion 8-bit operations per second per watt (TOPS/W) when executing conventional deep neural networks. Initially deployed at Sandia National Laboratories, Hala Point is designed to support research in brain-inspired artificial intelligence (AI) and aims to address challenges related to the efficiency and sustainability of current AI systems.

Neuro chips coming soon..

DEPARTMENTAL INFORMATIONS, EVENTS & AWARENESS PROGRAMS

PH.D AWARDEE (JUN25 -JULY25)

SOUMENDU GHOSH

- Thesis Title: **Design of Electromagnetic Metasurface for Polarization Engineering and Radar Stealth Applications**

Supervisor Name: **Dr. Abhishek Sarkhel**
Date of Award: **14/07/2025**

DEPARTMENTAL PROGRAM

- **B.Tech**
  - 2021-2025 Batch: 35
  - 2022-2026 Batch: 29
  - 2023-2027 Batch: 37
  - 2024-2028 Batch: 32
- **M.Tech**
  - 2023-2025 Batch: 02
  - 2024-2026 Batch: 12
- **Ph.D.**
  - Total: 30 (Full Time)

PUBLICATIONS

CONFERENCE, JOURNAL AND BOOK CHAPTERS

Journal

- *K. Vejandla et al., "Demonstration of a Novel SLM-Based PAPR Reduction Method for GFDM Using USRP Testbed," in IEEE Access, vol. 13, pp. 84399-84408, 2025, doi: 10.1109/ACCESS.2025.3568497.*
- *Gogoi K., et al., "A conceptual and simulation study on curved MOSFET based current mirror integrated pressure sensors (CM-CMIPS)," in Indian Journal of Engineering and Materials Sciences (IJEMS), Vol. 32, No. 01, 2025. https://doi.org/10.56042/ijems.v32i01.12111.*
- *Kumar, G., et al., "Analytical study on the SiC-MOSFET current mirror integrated MEMS pressure sensor for harsh environment applications," in Microsystem Technologies, 2025. https://doi.org/10.1007/s00542-025-05893-2*
- *Roy M, Basu S, Neogi B, Majumdar S, Saha P. Development and performance analysis of a human respiratory system using state-space model-based system identification technique. Microsystem Technologies. 2025 Jan 7:1-4.*
- *Roy M, Bhattacharjee S, Neogi B, Saha P. Design and development of an implantable circuit for adjusting required pressure inside of respiratory system. Microsystem Technologies. 2025 Feb;31(2):367-80.*
- *Ghosh, Soumendu, P. Megh Sainadh, Abhishek Sarkhel, and Saptarshi Ghosh. "Wideband Superstrate-Loaded Metasurface-based Multifunctional Polarization Converters,"IEEE Antennas Wireless propag lett., jan. 2025.*
- *Mukhopadhyay, Sunanda, Abhishek Sarkhel, Partha Pratim Sarkar, and Satyendra Singh Yadav. "Passive metasurface reflector for 6G wireless signal coverage enhancement in indoor environment: Design and experimental demonstrations." Physical Communication 71 (2025): 102664.*
- *Singh, Moirangthem Santoshkumar, Jeet Ghosh, Soumendu Ghosh, and Abhishek Sarkhel. "A compact dual-polarized triple-band antenna for implantable Biotelemetry applications." Journal of Electromagnetic Waves and Applications 39, no. 9 (2025): 1018-1034.*
- *Ghosh, Soumendu, P. Megh Sainadh, Abhishek Sarkhel, and Saptarshi Ghosh. "Wideband Superstrate-Loaded Metasurface-based Multifunctional Polarization Converters." IEEE Antennas and Wireless Propagation Letters (2025).*

Conference

- *J.Talukdar, Malvika, B.Das, K. Mummaneni, Performance Assessment of MoS2-Based Non uniform Tunnel Field Effect Transistors for Low-Power Applications Micro and Nanoelectronics Devices, Circuits and Systems, 2025 (presented).*
- *Mukhopadhyay, Sunanda, Abhishek Sarkhel, and Satyendra Singh Yadav. "A Wideband Digitally Coded Metasurface Using Staggering Tuning Mechanisms for Beam Steering Application in 6G mm-Wave Communication." In Millimeter Wave and Terahertz Devices for 5G and 6G Systems,. Springer, Nov 2025.(accepted)*
- *Suting, Habanaibok, Soumendu Ghosh, Abhishek Sarkhel, and Prabir Saha. "A Single-Layered Linear-to-Circular Polarization Converter for Dual-Band 5G Millimeter Wave Communications Systems Using Frequency Selective Surface." In Millimeter Wave and Terahertz Devices for 5G and 6G Systems,. Springer, Nov 2025.(accepted)*
- *Chattapadhyay, Debojyoti, Soumendu Ghosh, Satyendra Singh Yadav, and Abhishek Sarkhel. "A Polarization-Insensitive Triple Band Millimeter-Wave Absorber for 6G Radar Communication." In Millimeter Wave and Terahertz Devices for 5G and 6G Systems,. Springer, Nov 2025.(accepted)*
- *Mukhopadhyay, Sunanda, Kartikey Gupta, Anjali Kashyap, Abhishek Sarkhel, and Satyendra Singh Yadav. "Characteristics Analysis of 2-Bit Digitally Time-Coded Programmable Metasurface Using Vector Synthesis Approach." In 2024 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS), pp. 1-6. IEEE, 2024.*

RESEARCH AND DEVELOPMENT PROJECT

S. No	Name of the faculty member	Title of the Project	Period (From-To)	Sponsoring Organisation	Amount [INR]
1.	Dr. S. Majumdar.	Fully acoustics testing of low velocity impact damage in composite plate using the concept of local defect resonance	2022-25	Aeronautics R and D Board	24,02,800/-
2.	Dr. P. Rangababu, Dr. A. Sarkhel. Dr. S. K. Bandari, Dr. S. Majumdar, Dr. S. S. Yadav, Dr. P. K. Rathore, Dr. Prabir Saha, Dr. A. Dandapat.	AI Empowered Advanced Wireless Communication Systems	2021-2026	DST-FIST	80,00,000/-
3.	Dr. P. K. Rathore	Development of High Sensitivity CMOS-MEMS Integrated Pressure Sensor and System for Space Application	2019-2024	Indian Space Research Organisation (ISRO), Department of Space, Government of India	32,46,000/-
4.		Design and Development of Highly Sensitive Non-Conventional Ring Channel Shaped MOSFET Based Current Mirror Integrated Pressure Sensors	2021-2024	Department of Science & Technology, Ministry of Science and Technology, Government of India	44,93,601/-
5.	Dr. S. Majumdar	BRO Project - Sensor Based Big Data Analysis for Prognostics and Health Management of RCC Bridges	2023-2025	BRO	37,00,000/-
6.	Dr. P. Saha, Dr. P. K. Rathore, Dr. S. Majumdar.	SMDP Project - Development of On-chip MEMS Pressure Sensor based Tensiometer for Agriculture.	2023-2028	MIETY	1,10,00000/-
7.	Dr. P. Saha, Dr. A. Sarkhel, Dr. S. K. Bandari, Dr. S. Majumdar, Dr. S. S. Yadav.	TCIL Project- UAV Assisted Soil Moisture Content Determination through 5G Network	2023-2028	DoT	1,14,00000/-
8.	Dr. A. Sarkhel, Dr. S. S. Yadav.	Design and Development of Intelligent Reflecting Surface for Ubiquitous Connectivity Among IoT Enabled Devices	2025-2027	36,25,189	36,25,189/-

Editorial Board

Editor's

Dr. Salam Shuleenda Devi

Dr. Jagritee Talukdar

Members

Kalpana Gogoi
Roll No. P22EC004

Mahima Chaudhary
Roll No. P21EC002

Rabul Saikia
Roll No. P21EC003

Jintu Borah
Roll no. P21EC016

Seenivasan M A
Roll No. P21EC005

Debojyoti Chattapaddhyay
Roll No. P23EC002

James L Lyngkhoi
Roll NO. P24EC002

Marbaremdor Wahlang Pahsyntiew
Roll No. P23EC006

Contact us
Head of Department
hod.ec@nitm.ac.in

Electronics and Communication Engineering Department
National Institute of Technology Meghalaya
(An Institute of National Importance)