Patron

Prof. B. B. Biswal, Director, NIT Meghalaya

Organizing Chair

Dr.P.Rangababu, EC Dept. NIT Meghalaya

Convenors

Dr. P. Rangababu, NIT Meghalaya EC Dept.

Dr.Pradeep Kumar Rathore, NIT Meghalaya EC Dept

Members:

Faculties of EC Dept. NIT Meghalaya

Experts/Resource Persons

- **Shri. Israr Sheikh**, FAE Manager, India, ASEAN and ANZ, Intel–PSG
- **Shri. Padmanaban K**, Program Specialist –India, FPGA University Outreach, Intel–PSG
- **Prof. Shiva Prakash** Professor **IISC Bangalore &** NIT Meghalaya
- **Shri. Jose Simon Scientist-E, CDAC** Thiruvananthapuram.
- **Shri. Libin T T, Scientist- F, CDAC** Thiruvananthapuram
- **Shri. Rajesh, NIELIT Calicut**
- **Dr.Venu, Manjeera Digital Systems, Hyderabad**
- **Experts from NITS/other industries**

Who Can Register?

Faculty members of the technical institutions, Industry People, Research and PG scholars

Important Dates

Last date of application received	**1st Apr 2022**
Intimation of participation	**2nd Apr 2022**
Programme dates	**4th -8th April 2022**

How to Register

Interested participants may apply through online registration in link https://forms.gle/t5oQes3Kjcg7WuFu9 on or before **1st Apr 2022**.

- ***No registration fee*** will be charged from the participants.
- The number of participants is limited to 200.
- Participant's registration will be confirmed on first come first serve basis. Certificate will be issued to those participants who attend all the sessions online

Contact:

Dr. P. Rangababu, Department of Electronics and Communication, NIT Meghalaya, Shillong, Phone: +91 9485177063, Email: **custom_icdesign2021@nitm.ac.in**

Faculty Development Programme On

"Embedded System Design using FPGAs"

4th– 8th April 2022

Organized by

Department of Electronics and Communication Engineering
National Institute of Technology, Meghalaya

Venue

National Institute of Technology Meghalaya,
Bijni Complex, Laitumkhrah, Shillong, –793003

Course Objective

A modern custom IC chip is complex in nature; billions of transistors, millions of logic gates deployed for computation and control, along with large storage memories. How do engineers/researchers manage to design embedded systems for modern requirement of computation? Recent years have seen an increasing job market towards the Embedded system Design, VLSI Design. Working in these domains requires deep understanding of concepts and hands-on experience of Industry relevant Embedded system design, VLSI deign EDA Tools. This workshop focused on training the participants the (students/faculties/scholars/engineers) on the Intel IC design approaches, Embedded system design, High level synthesis, Timing analysis, verification etc.

About NIT Meghalaya

National Institute of Technology Meghalaya was established in the year 2010 as joint venture of Govt. of India and Govt. of Meghalaya with granted permanent campus of around 450 acres at Sohra Cherrapunjee. The institute is functioning in its temporary campus at Shillong in East Khasi Hills district of Meghalaya and is about 2 Kms from the main bus stand of Shillong on Police Bazaar – Laitumkhrah roadway. The city of Shillong is well connected with rest of country by road. The nearest railway station is at Guwahati (Assam), at a distance of 90 Kms from Shillong. The nearest airport is within city (15 Kms). The place has healthy climate with temperature ranging from 07°c to 16°c during December and is at an altitude of 1520 meters.

The Department of Electronics and Communication Engineering and Computer Science and Engineering was established in the year 2010. The Department offers B. Tech, M.Tech and Ph.D. programmes. The departments are well equipped with laboratories, computers, latest simulation softwares and our students are exposed to recent technologies and techniques. The departments have well experienced and dedicated faculty members with different research specializations in Microelectronics, VLSI Design and Embedded Systems, Communication, Digital Processing, RF Design Machine learning, Internet of Things etc

Program Contents

- Intel FPGA Portfolio and Quartus Software
- Timing Analysis and Timing Closure
- Intel SoC FPGAs
- High Level Synthesis and Intel FPGAs for AI
- High Speed I/0
- Design of Realtime Embedded systems
- Plenary Discussion
- CDACs Vega processor
- FPGA-based SoC system

National Institute of Technology Meghalaya, Bijni Complex, Shillong-793003

Course Schedule

Dates	9.30AM to 11:00AM	11:05 AM to 11.15AM	11.15AM to 1:00 PM	1.15 PM to 2:00 PM	2:00 PM to 3.30 PM
04.04.2022 (Monday)	Registration and Inauguration & **Session 1** Intel FPGA Portfolio Shri. Israr Sheikh Intel	Tea	**Session 2** Quartus tool flow and lab demo, Shri. Padmanaban	Lunch	**Session 3** VEGA processors & Ecosystem Shri. Libin T T SC-F CDAC Thiruvanathapuram
05.04.2022 (Tuesday)	**Session 4** Timing closure on Intel FPGA Shri. Padmanaban, Intel	Tea	**Session 5** Timing closure on Intel FPGA lab Shri. Padmanaban, Intel	Lunch	**Session 6** Talk: Dr. K.Venu Manjeera Digital Systems
06.04.2022 (Wednesday)	**Session 7** Intel SoC FPGAs Shri. Padmanaban, Intel	Tea	**Session 8** Intel SoC FPGAs Lab Shri. Padmanaban, Intel	Lunch	**Session 9** FPGA based SoC Design Shri. Jose Simon SC-E CDAC Thiruvanathapuram **&** **Session 10** A plenary discussion: Chairman: Prof Shiva Prakash, Professor, Shri Jose Simon SC-E, CDAC Shri. Padmanaban, Intel
07.04.2022 (Thursday)	**Session 11a** High Level Synthesis and Intel FPGAs for AI Shri. Padmanaban, Intel	Tea	**Session 11b** High Level Synthesis and Intel FPGAs for AI lab Shri. Padmanaban, Intel	Lunch	**Session 12** Talk by Shri. Rajesh M NIELIT Calicut
08.04.2022 (Friday)	**Session 13a** High Speed I/0 Shri. Padmanaban, Intel	Tea	**Session 13b** High Speed I/0 Lab Shri. Padmanaban, Intel	Lunch	**Session 14** Talk by Dr.Rangababu/Dr.Shubankar Majumdar, NIT Meghalaya